Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WENYAN JIA and BORIVOJE NIKOLIC

Appeal No. 2002-0142
Application No. 09/248,957

HEARD: March 5, 2003

Before FLEMING, SAADAT, and LEVY, Administrative Patent Judges.
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-8, which are all of the claims pending in this application.

BACKGROUND

Appellants' invention relates to a sense amplifier-based flip-flop with asynchronous set and reset. An understanding of the invention can be derived from a reading of exemplary claims 1 and 8, which are reproduced as follows:

1. A flip-flop for asynchronous set and reset, comprising:

a first stage for inputting a differential set of data inputs and generating a differential set of outputs;

a set and reset second stage for receiving said set of differential set of outputs from said first stage and to output a differential set of outputs including *a Q* signal and a *Q* signal from said set and reset second stage, wherein said signal *Q* and signal *Q* have equal delay times.

8. A flip-flop for asynchronous set and reset, comprising:

a first stage for inputting a differential set of data inputs and generating a differential set of outputs, said outputs being a set signal and a reset signal;

a set and reset second stage for receiving said set of differential set of outputs from said first stage and to output a differential set of outputs including a *Q* signal and a *Q* signal from said set and reset second stage; and

a circuit to provide asynchronous operation of said set and reset signals and to prevent short circuit connection when *Set* and *Clear* [1]are asserted.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Sato	5,532,634	July 2, 1996

Claims 1-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sato.

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[1] Although we find no clear antecedent basis for "Set and Clear, because the metes and bounds of the claim are readily understandable, we consider this to be a formal matter that can be addressed by the examiner subsequent to the appeal.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejection, we make reference to the examiner's answer (Paper No. 15, mailed April 10, 2001) for the examiner's complete reasoning in support of the rejection, and to appellants' brief (Paper No. 13, filed February 15, 2001) for appellants' arguments thereagainst. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejection advanced by the examiner, and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

Upon consideration of the record before us, we reverse.

To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997). As stated in In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) (quoting Hansgirg v. Kemmer, 102 F.2d 212, 214, 40 USPQ 665, 667 (CCPA 1939)) (internal citations omitted):

> "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. If, however, the disclosure is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient."

We consider first the rejection of claim 1 based upon the teachings of Sato. Appellants assert (brief, pages 8 and 9) that Sato does not disclose that the signal Q and the signal Q have equal delay times as required by claim 1. It is argued (id.) that in appellants' invention, the output stage includes a pull-up circuit and a pull-down circuit, and that the circuits are symmetrical with respect to the first and second current paths, resulting in equal delay times. Appellants direct our attention to page 12 of appellants' specification which discloses that as a result of the symmetrical design, the rising and falling edge

signals Q and Q are subject to the same delays. The examiner alleges (answer, page 3 referring to the final rejection, paper No. 8, and answer, pages 4, 6 and 7) that the time delay of the Q signal in figure 7 of Sato is inherently equal to the time delay of the Q signal because Sato's circuit has a symmetric structure. Appellants argue (id.) that in figure 7 of Sato, "elements 29 and 44 are arranged significantly differently than elements 42 and 38. there is no symmetrical design and, consequently, no equal delay times. Because of the different arrangement, there is no inherency."

The examiner responds (answer, page 7) that since transistor 29 operates only during synchronous operation mode and transistors 38, 42 and 44 only operate during asynchronous set and reset mode, that appellants' arguments drawn to the symmetry feature of these transistors is not a valid comparison.

From our review of Sato, we find no support for the examiner's assertion that transistors 38, 42, and 44 operate in asynchronous set and reset modes. We find that N-MOSFETS 35-38 were added to the embodiment of figure 3 to provide a set input function to flip-flop circuits 1 and 2 (see figure 5, and col. 7., lines 1-5) and that N-MOSFETS 41-44 have been added in the embodiment of figure 3 to provide a reset input function to the

flip-flop circuits 1 and 2 (see figure 6 and col. 7, lines 26-29). We agree with appellants that as shown in figure 7, referred to by the examiner, elements 29 and 44 are arranged significantly differently than elements 42 and 38, and therefore do not establish that signal Q and signal Q have equal delay times. We are not persuaded by the examiner's (answer, pages 6 and 7) choosing from the circuit of figure 7, portions of the circuit that also pertain to the circuit of figure 3, in an attempt to read Sato on the claimed invention. In sum, we find that the examiner has failed to point to any showing in Sato that establishes equal delay times for the signals Q and Q. From all of the above, we find that the examiner has failed to establish a prima facie case of anticipation of claim 1. Accordingly, the rejection of claim 1 under 35 U.S.C. § 102(b) is reversed.

We turn next to independent claims 5-8. The issue with respect to these claims relates to a circuit to provide asynchronous operation of the "first stage" (claim 5), "set signal" (claim 6), "reset signal"(claim 7), and "set and reset" signals (claim 8). Beginning with claim 5, appellant asserts (brief, page 9) that inverters 40 and 45 and transistors 35, 37, 41, and 43, relied upon by the examiner (answer, page 5), are dependent upon the next clock signal CL2, and consequently, the

circuit is not asynchronous." The examiner responds (answer, page 7) asserting:

> However, Sato teaches on column 7, lines 18-25 that when the set signal S goes "H", transistor 35 is turned ON and transistor 37 is turned OFF, node 3(BP) goes "L" and node 4(P) goes "H" **regardless of the clock signal CL2, i.e., the first stage is not dependent on the next clock signal CL2 when the set signal S is asserted** (emphasis added).
>
> On column 7, lines 45-52, Sato teaches when the reset signal R goes "H", transistor 41 is turned ON and transistor 43 is turned OFF, node 3(BP) goes "H" and node 4 (P) goes L" **regardless of the clock signal CL2, i.e., the first stage is dependent on the next clock signal CL2 when the reset signal is asserted** (emphasis added).

From our review of Sato, we find that Sato discloses that in prior art circuit arrangements, the J and K inputs are fetched by the master flip-flop through an inverter operation in response to clock pulses CP and BCP or a gate operation in response to the clock pulses ϕ1 and ϕ2, and are shifted to the slave flip-flop to obtain the outputs Q and BQ (col. 1, lines 48-54). Problems associated with these circuits are that they result in a high cost large scale integration (LSI), increased area of the circuit, and these circuits are not suitable for high speed operations (col. 1, line 55 through col. 2, line 6). It is an object of the invention to reduce the number of elements in the circuit, and to provide circuit means for supplying a logic output of a control signal to a flip-flop circuit without using any CMOS gate circuits (col. 2, lines 23-30 and 58-62). Sato

further discloses (col. 2, lines 30-39) that to achieve the object of the invention, there is provided a J-K flip-flop circuit having first and second flip-flop circuits constituted by connecting inputs and outputs of two CMOS inverters to each other, first NAND type connection means in which one end of three MOS transistors, which respectively receive a first clock, a J signal, and a signal from one node of the second flip-flop at their gates, and have current paths connected in series with each other. Sato further discloses (col. 2, lines 36-39) that one end of the 3 MOS transistors:

> is connected to one node of the first flip flop circuit; second NAND type connection means in which one end of three MOS transistors, which respectively receive the first clock, a K signal, and a signal from the other node of the second flip-flop circuit at their gates, and have current paths connected in series with each other, is connected to the other node of the first flip-flop circuit.

The portions of Sato relied upon by the examiner to support the examiner's assertion of asynchronous operation of the first stage, as well as asynchronous set and reset functions are as follows (col. 7, lines 18-25 and lines 45-52):

> According to the arrangement shown in FIG. 5, when the set signal S goes to “H”, the N-MOSFETs 35 and 36 are turned on, and the N-MOSFETs 37 and 38 are turned off. Therefore, since the node 3 goes to “L”, the P-MOSFET 13 is turned on, and the node 4 goes to “H”. On the other hand, since the node 5 (BQ) goes to “L”, the P-MOSFET 17 is turned on, and the node 6 (Q) goes to “H”. In this manner, a set state is established.

> According to the arrangement shown in FIG. 6, when the reset signal R goes to "H", the N-MOSFETs 41 and 42 are turned on, and the N-MOSFETs 43 and 44 are turned off. Therefore, since the node 4 goes to "L", the P-MOSFET 11 is turned on, and the node 3 goes to "H". On the other hand, since the node 6 (Q) goes to "L", the P-MOSFET 15 is turned on, and the node 5 (BQ) goes to "H". Thus, a reset state is established.

From our review of Sato, we find no disclosure of Sato teaching asynchronous operation of the first stage, or the set and reset functions, as advanced by the examiner. The initial burden of establishing a prima facie case rests with the examiner. Here, the language of the portions of Sato relied upon do not support the examiner's position as quoted, supra, and we therefore agree with appellants that the operations of the circuits of figures 6-8 of Sato are synchronous, i.e., clock driven. Accordingly, we find that the examiner has failed to establish a prima facie case of anticipation of independent claim 5. As the examiner (answer, pages 8 and 9) relies upon the same portions of Sato for the other independent claims, we find that the examiner has not established a prima facie case of anticipation of claims 7 or 8. Accordingly, the rejection of claims 1-8 under 35 U.S.C. § 102(b) as anticipated by Sato is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-8 under 35 U.S.C. § 102(b) is reversed.

REVERSED

MICHAEL R. FLEMING Administrative Patent Judge	)
MAHSHID D. SAADAT Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)

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